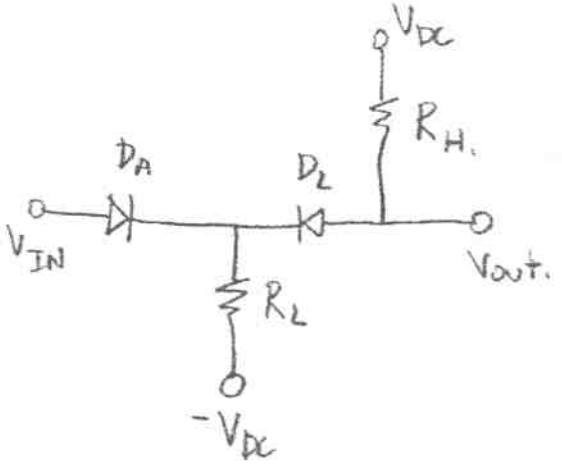
— HW #3 —

(EE 282)

Due: April 08, 2011 (Friday)

① Sketch VTC of the following Circuit:



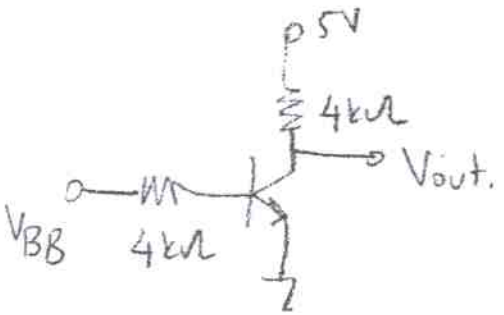
$-V_{DC} < V_{IN} < V_{DC}$

$V_{DC} = 4V$

$R_H = R_L = 1k\Omega$

$V_D(ON) = 0.7V$

② Sketch VTC and find noise margins of the following gate:

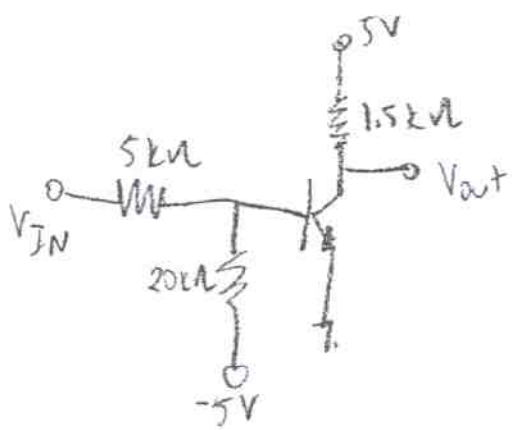


$\beta_F = 100$

$V_{BE(FA)} = V_{BE(SAT)} = 0.7V$

$V_{CE(SAT)} = 0.2V$

③ Sketch VTC and noise margins.



$\beta_F = 100$;

$V_{BE(FA)} = 0.7V$;

$V_{BE(SAT)} = 0.75V$;

$V_{CE(SAT)} = 0.1V$;