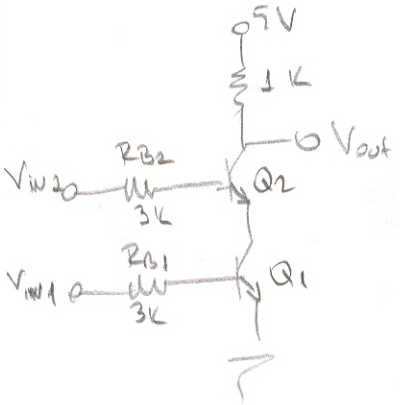
EE282
Homework # 4
Solutions

Q.1.



i) a) $V_{IN1} = V_{IN2} = 0$ V : Both Q_1 & Q_2 are CUT OFF. Therefore

$I_{B1} = I_{B2} = I_{RC} = 0$ $\quad V_{OUT} = V_{CC} = 5V$

b) $V_{IN1} = 0V$, $V_{IN2} = 5V$: Both Q_1 & Q_2 are CUT OFF. Therefore

$I_{B1} = I_{B2} = I_{RC} = 0$ $\quad V_{out} = V_{CC} = 5V$

c) $V_{IN1} = 5V$, $V_{IN2} = 0V$: Q_1 is in SATURATION
Q_2 is CUT OFF.

Q_1 is in SATURATION mode since :

$I_{C1} = I_{E2} = 0$ $\quad \beta_F I_{B1} > I_{C1} = 0$

and

$$I_{B1} = \frac{5 - 0.8}{3} = \frac{4.2}{3} = 1.4 \text{ mA}, \quad I_{B2} = 0, \quad I_{RC} = 0$$

$$V_{out} = V_{CC} - R_C \cdot I_{RC} = V_{CC} = 5V$$

d) $V_{IN1} = 5V$, $V_{IN2} = 5V$: Both Q_1 and Q_2 are in SATURATION mode.

$$V_{C1} = V_{E2} = V_{CE(SAT)} = 0.2 \text{ V}$$

$$V_{C2} = V_{OUT} = V_{E2} + V_{CE(SAT)} = 0.2 + 0.2 = 0.4 \text{ V}$$

$$I_{B1} = \frac{5 - 0.8}{3K} = \frac{4.2}{3K} = 1.4 \text{ mA}$$

$$I_{B2} = \frac{5 - (V_{E2} + V_{BE(SAT)})}{3K} = \frac{5 - (0.2 + 0.8)}{3K} = \frac{4}{3} = 1.33 \text{ mA}$$

$$I_{RC} = \frac{5 - V_{OUT}}{1K} = \frac{5 - 0.4}{1K} = \frac{4.6}{1K} = 4.6 \text{ mA}$$

ii. If logic 0 is represented by 0V and logic 1 is represented by 5V then this is a NAND Gate.

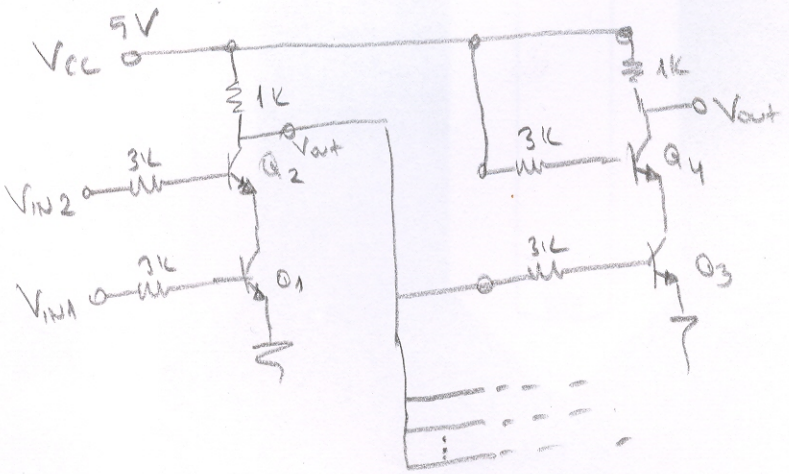
V_{IN1} (V)	V_{IN2} (V)	V_{OUT} (V)
0	0	5
0	5	5
5	0	5
5	5	0.4

iii.

a) First consider the low output case, namely both Q_1 & Q_2 are in SATURATION mode. Therefore, $V_{OUT} = 0.4$ V and all the transistors of the following stages connected to V_{OUT} terminal are CUT OFF. Since these transistors require no base current from the previous stage, there exists no limitation for the number of NAND gates that can be driven by a NAND gate.

b) Now consider the high output case, namely atleast Q_2 among Q_1 & Q_2 is CUT OFF. Base current of following stages is supplied by I_{RC}. If N is the number of NAND gates driven by the first stage NAND gate then,

$$I_{RC} = N \times I_B \quad , \quad N = \frac{I_{RC}}{I_B}$$



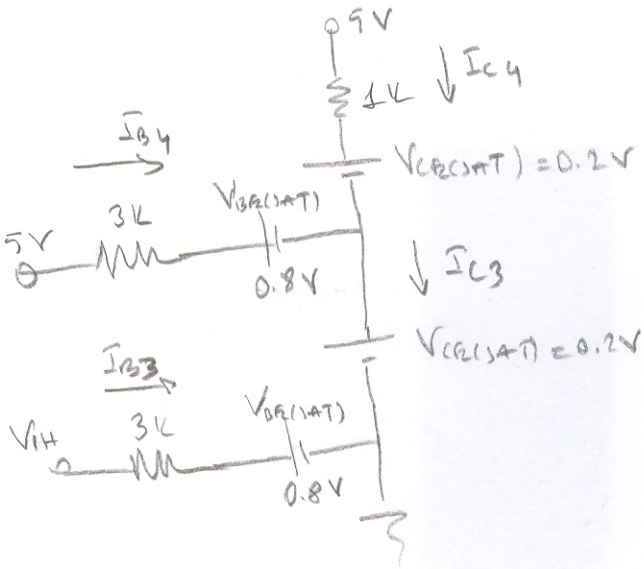
To get the fan-out, one must maximize I_{RC} and minimize I_B. So we need to express I_{RC} and I_B explicitly:

$$I_{RC} = \frac{V_{CC} - V_{out}}{R_C} \quad , \quad I_B = \frac{V_{out} - V_{BE(SAT)}}{R_B}$$

Only adjustable parameter in the above expression is V_{OUT}. V_{OUT} must be set to its lowest possible value in order to obtain a maximum I_{RL} and a minimum I_B. For proper operation of logic gates following condition must be satisfied:

$$V_{OUT} \geq V_{IH}$$

where V_{IH} is the high level input voltage and can be calculated by considering the transistor Q_4 to be in SATURATION and the transistor Q_3 to be in the edge of saturation region:



First calculate base and collector currents of transistors Q_3 & Q_4

$$I_{B4} = \frac{5 - 0.8 - 0.2}{3K} = \frac{4}{3K} = 1.33 mA$$

$$I_{C4} = \frac{5 - 0.2 - 0.2}{1K} = 4.6 mA$$

$$I_{B3} = \frac{V_{IH} - 0.8}{3K} = \frac{I_{C3}}{\beta_f} = \frac{I_{B4} + I_{C4}}{\beta_f}$$

$$= \frac{1.33 + 4.6}{20} = \frac{5.93}{20} = 0.2965 mA$$

$$\Rightarrow V_{IH} = 0.8 + 3 \cdot 0.2965 = 1.6893 V$$

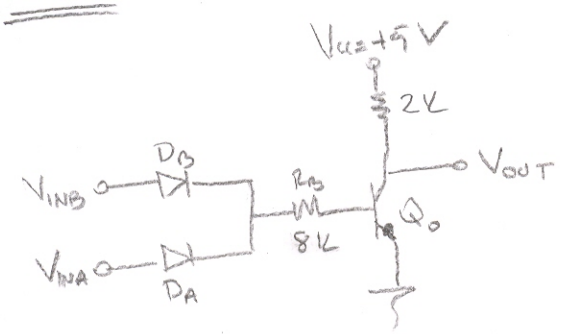
To make the fan-out maximum, V_{OUT} must be equal to its lowest possible value:

$$V_{OUT} = V_{IH} = 1.6893 V$$

$$N = \frac{I_{RL}}{I_B} = \frac{\frac{(5 - 1.6893)}{1K}}{0.2965} = 11.16$$

Maximum fan-out is 11.

9.2



i. (1) * $V_{INA} = V_{INB} = 0\ V$

Diode D_A and D_B are OFF.

Q_0 is CUT OFF

Therefore, $V_{OUT} = V_{CC} = 5\ V$

(2) * $V_{INA} = 0$ $V_{INB} = 5V$

D_A is OFF, D_B is ON

Q_0 is in SATURATION mode. Therefore

$V_{OUT} = V_{CE(SAT)} = 0.2\ V$

(3) * $V_{INA} = 5\ V$ $V_{INB} = 0\ V$

D_A is ON D_B is OFF

Q_0 is in SATURATION mode

Therefore, $V_{OUT} = V_{CE(SAT)} = 0.2V$

(4) * $V_{INA} = V_{INB} = +5\ V$

D_A and D_B are both ON.

Q_0 is in SATURATION mode

$V_{OUT} = V_{CE(SAT)} = 0.2\ V$

$V_{INA}(V)$	$V_{INB}(V)$	$V_{OUT}(V)$
0	0	5
0	5	0.2
5	0	0.2
5	5	0.2

If logic 0 is represented by 0 and logic 1 is represented by 5 V, then this gate is a NOR gate.

ii

(1) $V_{IN} = 0V$ diodes D_A & D_B are OFF and Q_0 is CUT OFF since

$V_{IN} < V_{D(ON)}$, $V_{IN} < V_{BE(FA)}$

for this case the output voltage is

$V_{OUT} = V_{OH} = V_{CC} - R_C \times I_{RC} = V_{CC} = 5V$, since $I_{RC} = 0$

(2) When V_{IN} is increased to

$V_{IN} = V_{IL} = V_{D(ON)} + V_{BE(FA)} = 0.7 + 0.7 = 1.4\ V$

Both diodes D_A & D_B are ON, and Q_0 just enters FORWARD ACTIVE region from CUT OFF. The output voltage expression as a function of V_{IN} is as follows

$$V_{OUT} = V_{CC} - R_C I_{RC}$$
$$= V_{CC} - R_C \cdot \beta_f I_B$$
$$= V_{CC} - R_C \cdot \beta_f \frac{V_{IN} - V_{D(ON)} - V_{BE(FA)}}{R_B}$$

(3) As V_{IN} is increased to V_{IH}, Q_0 just enters SATURATION region from FORWARD ACTIVE region. For this case the output voltage is as follows:

$$V_{OUT} = V_{OL} = V_{CE(SAT)} = 0.2\ V$$

Now, calculate V_{IH}:

$$I_C = \frac{V_{CC} - V_{OUT}}{R_C} = \frac{V_{CC} - V_{CE(SAT)}}{R_C}$$

$$I_B = \frac{V_{IN} - V_{D(ON)} - V_{BE(SAT)}}{R_B} = \frac{V_{IH} - V_{D(ON)} - V_{BE(SAT)}}{R_B}$$

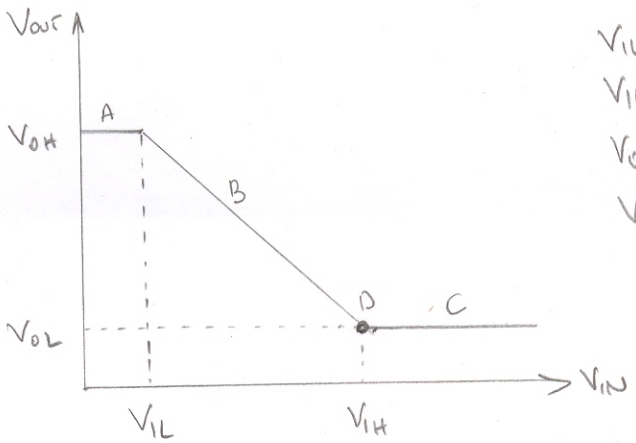
Since Q_0 is at the edge of saturation also we can relate I_B and I_C to each other as follows:

$$I_B = \frac{I_C}{\beta_f} = \frac{V_{IH} - V_{D(ON)} - V_{BE(SAT)}}{R_B} = \frac{V_{CC} - V_{CE(SAT)}}{\beta_f R_C}$$

$$\Rightarrow V_{IH} = V_{D(ON)} + V_{BE(SAT)} + \frac{R_B}{\beta_f R_C}(V_{CC} - V_{CE(SAT)})$$

$$= 0.7 + 0.8 + \frac{8K}{100 \times 2K}(5 - 0.2) = 1.5 + \frac{4}{100}(4.8) = 1.692\ V$$

A : Q_0 is CUTOFF
B : Q_0 is in FA
C : Q_0 is in SATURATION
D : Q_0 is at the edge of SATURATION



$V_{IL} = 1.4\ V$
$V_{IH} = 1.692\ V$
$V_{OL} = 0.2\ V$
$V_{OH} = 5\ V$

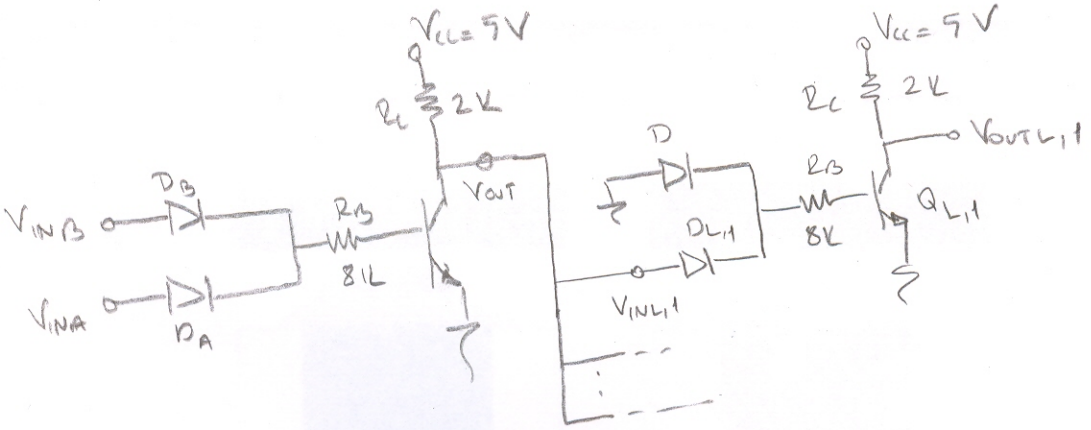
iii High noise margin is as follows:

$$V_{NMH} = V_{OH} - V_{IH} = 5 - 1.692 = 3.308$$

The low noise margin is as follows:

$$V_{NML} = V_{IL} - V_{OL} = 1.4 - 0.2 = 1.2\ V$$

iv



a) First consider the low output case, namely $V_{OUT} = 0.2\ V$. For this case all diodes ($D_{L,i}$) of the following stage are OFF and also $Q_{L,i}$ are CUT OFF. Since transistors of the following stages require no current there is no limitation for the number of stages that can be connected.

b) Now consider the high output case, namely at least one of D_A or D_B is ON. Similar to Q1 part iii, all the base currents of the transistors of the following stage is supplied by I_{RC}. Let N be the number of stages to be connected to the original DTL circuit. Then,

$$I_{RC} = N \times I_B \Rightarrow N = \frac{I_{RC}}{I_B}$$

I_{RC} and I_B can be expressed as follows

$$I_{RC} = \frac{V_{CC} - V_{OUT}}{R_C}, \quad I_B = \frac{V_{OUT} - V_{D(ON)} - V_{BE(SAT)}}{R_B}$$

For proper operation of logic gates the following relation must be satisfied

$$V_{OUT} \geq V_{IH}$$

To maximize the number of stages to be connected to the original DTL circuit V_{OUT} must be equal to V_{IH}. Now N can be calculated as;

$$N = \frac{I_{2C}}{I_B} = \frac{R_B}{R_L} \frac{V_{CC} - V_{OUT}}{V_{OUT} - V_{D(ON)} - V_{BE(SAT)}}$$

$$= \frac{R_B}{R_L} \frac{V_{CC} - V_{IH}}{V_{IH} - V_{D(ON)} - V_{BE(SAT)}}$$

$$= \frac{8k}{2k} \frac{5 - 1.692}{1.692 - 0.7 - 0.8}$$

$$= 4 \cdot \frac{3.308}{0.192} = 68.91$$

Fan_out is 68 for this DTL gate